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Quantitative strain measurement in 45-65nm CMOS transistors by energy-filtered convergent beam electron diffraction at low temperature

L. Clément [a,*], **R. Pantel** [b], **P. Morin** [b], **L. Kwakman** [a], **C. Wyon** [c]

[a] *NXP SEMICONDUCTORS, 860 rue Jean Monnet, F-38920 CROLLES, FRANCE*
[b] *STMICROELECTRONICS, 850 rue Jean Monnet, F-38926 CROLLES, FRANCE*
[c] *CEA-LETI MINATEC, 17 rue des Martyrs, F-38054 GRENOBLE, FRANCE*

Abstract – The Convergent Beam Electron Diffraction (CBED) technique is used here to determine the strain and stress state in the silicon channel gate of latest generation transistors. To improve the accuracy of the quantitative CBED strain analysis, cooling of the TEM sample by using liquid nitrogen is proposed. The results obtained on transistors stressed by two different processes are presented.

1. Introduction

Strain in CMOS transistor channels can be induced by an uniaxial stressed Si_3N_4 Contact Etch Stop Layer (CESL) deposited on the top of the transistor gates or by selective epitaxial growth of SiGe source/drain (S/D) regions. These types of stressors are used to increase the electron and hole mobility and thus to enhance the transistor switching speed.

A great challenge in the process development of such devices is to control the applied stress. Characterization techniques are needed to quantitatively measure stress or strain with a spatial resolution coherent with devices dimensions, that is to say, with a nanometre spatial resolution.

Convergent Beam Electron Diffraction (CBED) in a Transmission Electron Microscope (TEM) appears to be one of the most powerful techniques for local strain measurement with a resolution of about 1 nm. From the experimental HOLZ lines positions the local lattice parameters can be obtained and the strain in the crystal can be determined with a sensitivity of $2\ 10^{-4}$ [1].

Nevertheless, the main drawback of all TEM derived techniques relates to the thin TEM lamella preparation which induces stress relaxation at the created free surfaces. CBED patterns can be disturbed due to a non uniform strain across the specimen. Varying Bragg conditions along the electron beam path induce HOLZ lines broadening and the processing of such patterns becomes more complex [2]. We have already shown that when combining finite element modeling of this stress relaxation in the TEM lamella with dynamical electron diffraction, HOLZ lines broadening can be reliably reproduced. Based on these findings, we propose an original procedure for strain measurement in complex devices through the quantification of stress relaxation in a TEM sample [3].

In this work, only CBED patterns with fine (non-broadened) HOLZ lines are analyzed. As a matter of fact, in some cases, due to specific device geometry, such patterns can be obtained and a classical approach for strain measurement can then be used.

In order to enhance the sensitivity and especially for improving the numerical extraction of experimental HOLZ lines by the Hough transform algorithm, we propose to cool down the sample with liquid nitrogen. By doing so, the diffracted intensity is increased while the background intensity is decreased. Hence, the signal to noise ratio is improved and HOLZ lines extraction is easier.

2. Instrumentation and specimen preparation

The present studies were performed on a FEI TECNAI F20 TEM equipped with a Gatan Imaging Filter (GIF 2000). The microscope was operated at a nominal high-voltage setting of 200kV. The STEM CBED mode was used which allows to obtain a small probe size (1nm) with sufficient intensity.

Inelastically scattered electrons were eliminated using an energy selecting slit with a width of 20eV centered on the zero-loss peak. CBED patterns were acquired along a direction close to the [340] zone axis which is about 8.4° off the [110] cross section**.** In order to get sharper and better resolved HOLZ lines, a liquid-nitrogen cold stage was used to cool down the sample to ~ 100 K. TEM samples were prepared in-situ in a FEI DB400 Dual Beam machine combining Focused Ion Beam (FIB) and Scanning Electron Microscope (SEM) columns.

3. Results

Figure 1 shows CBED results obtained in periodic transistors on top of which a tensile nitride liner has been deposited which induces tensile strain in the silicon channel. The experimental CBED patterns acquired at different depths under the gate clearly indicate a transition from a strain-free to a tensile strain state in the silicon channel. After extraction of the lattice parameters we apply a dynamical simulation of the full CBED pattern, this to further enhance the accuracy of the determination of the HOLZ line shifts and, thus, of the quantification of the strain in the device.

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[*] Author to contact : laurent.clement@nxp.com – Tel : 04 38 92 35 01

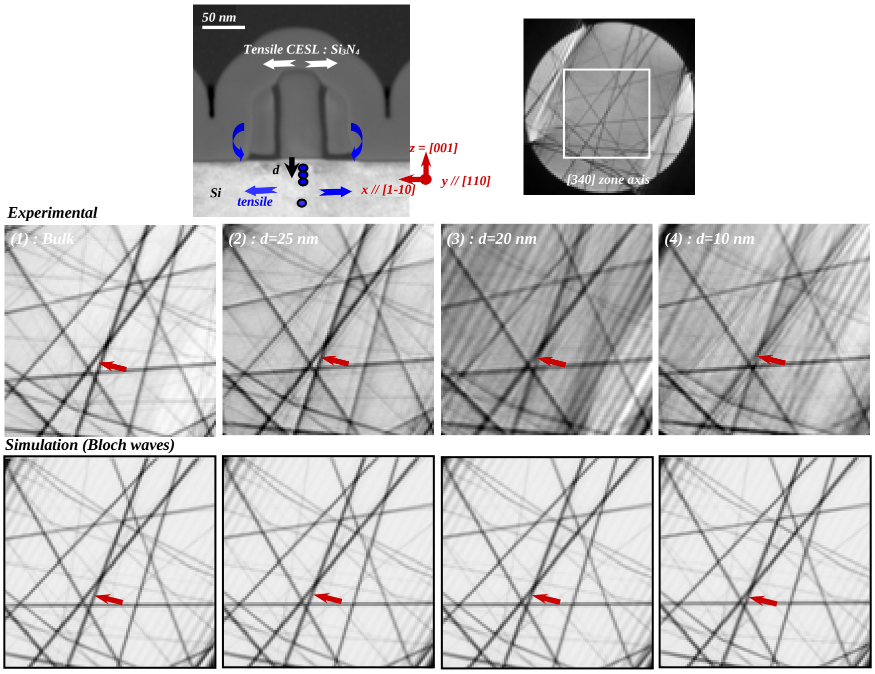

Figure 1 – Experimental CBED patterns acquired at different depths d under the gate. The change in HOLZ lines intersection (indicated by red arrows) reproduced by N-beams dynimical simulation reveals tensile strain in silicon channel due to nitride liner deposition on the top of the gate.

The second example given relates to the stress investigation in a complete transistor with a gate length ~ 50 nm and with epitaxially grown SiGe source and drain regions (Fig. 2). Once again, a change in the HOLZ lines positions is observed. In this case, the simulation results indicate a compressive stress state in the silicon channel gate.

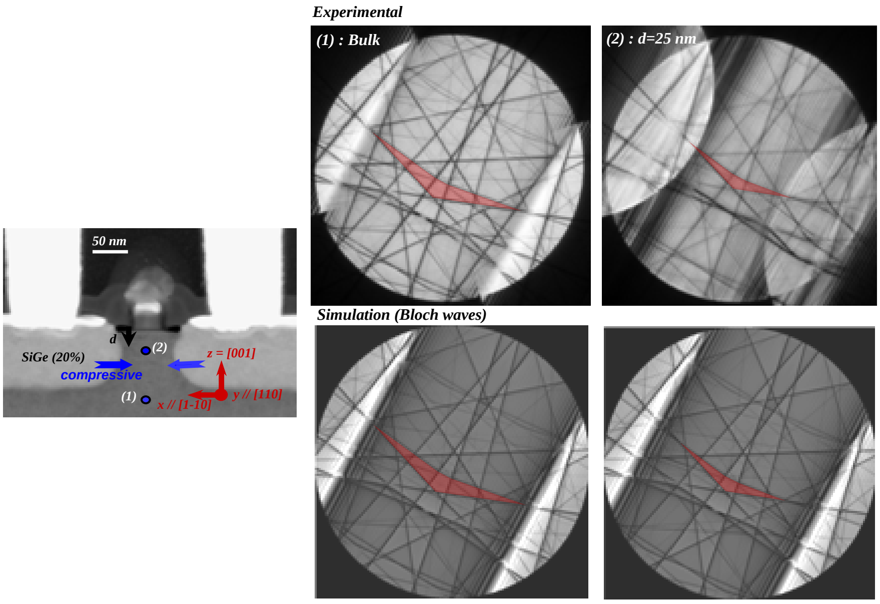

Figure 2 – Application of the CBED technique on complete transistor integrating epitaxially grown SiGe source and drain regions. Compressive stress state of silicon cristal between source and drain is visible in experimental CBED patterns and confirmed by dynamical simulation.

4. References

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