Structural properties of gold catalyzed silicon nanowires: Defects in the wires and gold on the wires

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Silicon nanowires were grown by the Vapour-Liquid-Solid (VLS) mechanism using gold as the catalyst and silane as the precursor. Although the crystalline quality of the wires is very high, sometimes defects can be observed. Some examples are shown. Gold clusters were observed on the lateral sides of the wires by means of STEM (Scanning Transmission Electron Microscopy), EDX (Energy Dispersive X-ray) analysis and SEM (Scanning Electron Microscopy) images. An approximate calculation shows that the nanowire sidewalls are covered by one monolayer of gold during growth. De-wetting of the monolayer after growth results in a homogenous distribution of gold clusters on the lateral surfaces of the wires.

1. Introduction

Silicon nanowires have been actively studied the last decade, as they held the promise of becoming key building blocks in future electronic and opto-electronic devices. They are compatible with silicon technology and could be most elegantly grown directly on their final position in a device on a wafer. However successful integration of nanowires in devices will depend ultimately on the degree of control that can be obtained over structure and physical properties. Nanowires were long time regarded as perfect crystals with straight sidewalls. Only recent publications have shown that faceting is actually a rather common phenomenon. This can be caused by regular twinning [1], or by the absence of a vertical low energy plane [2]. Defects in the nanowires or traces of (gold) catalyst on the nanowire sidewall, can change its physical properties. The wires studied in here generally contained few defects. Because the observation of a defect was limited to incidents, we will characterize these defects, but are unable to provide a more general model.

Furthermore we show evidence of gold rich clusters on the lateral surfaces of silicon nanowires and characterize these clusters. Convincing indirect evidence was presented by Hannon et al [3], proving the presence of gold on lateral surfaces of silicon nanowires. Furthermore Werner et al [4] showed gold clusters on silicon wires grown by MBE. However the wires described in these publications were all grown under ultra high vacuum conditions, partially to allow in situ observation. The wires presented in this work are not grown under UHV. Pan et al [5] reported the presence of gold-rich precipitates on boron doped silicon nanowires. These precipitates seem to be preferentially present on the highly doped regions of the wires. The gold precipitates are explained by instabilities at the liquid/solid interface, caused by the addition of the dopant gas flow. Since we regard only undoped samples this explanation is insufficient. Our experiments do not provide evidence that gold also contributes to the faceting, as suggested by Ross et al [2], we just note that gold is unambiguously present on the lateral faces of all observed nanowires, which genereally also showed the same type of facting.

2. Results

Generally the Crystalline quality of the wires is high and few defects can be observed. Large wires ($r > 20$ nm) grow in the <111> direction [6] and can sometimes contain horizontal twins near the base or at a kink. Figure I shows some examples. One kink was observed without a grain boundary. In this case, the kink was caused by growth along one of the three inclined <111> direction. Smaller wires ($r < 20$ nm) sometimes contain a vertical defect. A vertical twin in a [112] oriented nanowire and an "incommensurate$\sqrt{2}$" Si(100)/Si(0-11) domain in a [011] oriented nanowire were incidentally observed (not shown).

In Figure II STEM images of a Silicon nanowire, and EDX measurements at the same wire, are shown. Brighter regions can be observed on the wire and facets can be distinguished. An arrow indicates where the EDX spectra has been taken. The EDX measurements on different parts of the wire show that the brighter particles are gold rich clusters. Analysis of the clusters reveals an average diameter of 3-4 nm and a thickness of 2 nm, being approximately 4 to 5 monolayers of gold. These clusters can be observed in SEM as well (not shown). STEM and SEM images show that approximately 20% of the wire surface is covered by gold clusters. This implies that during growth the lateral faces of the wire will be covered by approximately one monolayer of gold. This figure is in good agreement with the value found by Hannon et al [3]. De-wetting of the monolayer occurs after growth resulting in observed clusters. In Figure III a high resolution TEM image of the wire sidewall faceting is shown, as also observed by [2]. Vector calculation allows identifying the alternating planes as shown.

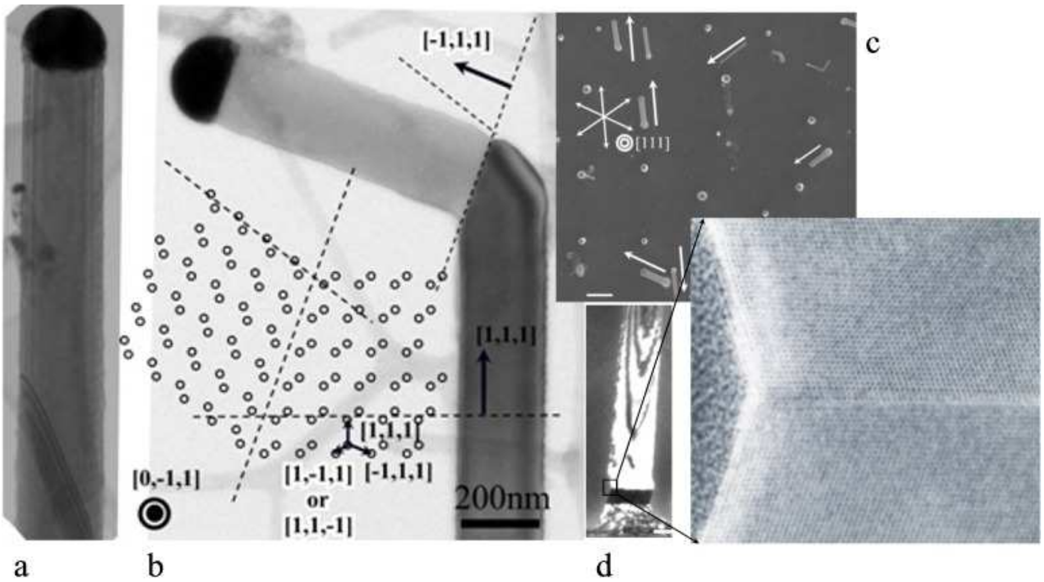
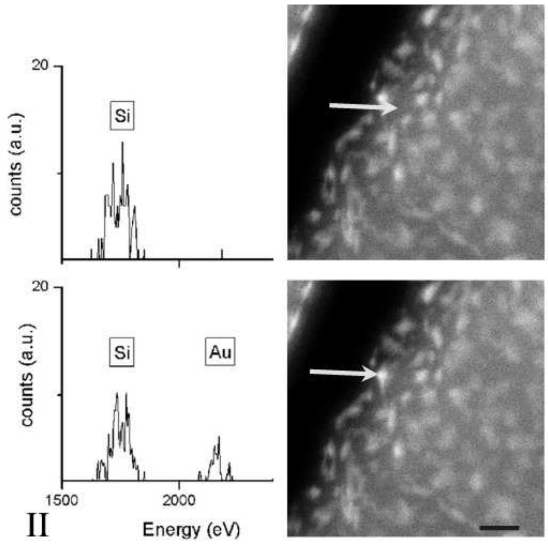


Figure I – *Relatively large (r > 20 nm) nanowires containing one or more twins. (a b) Conventionnal two beam TEM images. (a) Showing a stacking fault on an inclined {111} plane. (b) Kinked nanowire. Reconstruction of the lattice shows the kink is caused by a sigma = 3 twin fault on a <111> plane. Growth continous in a <111> direction. (c) SEM top view showing that this kind of defect can be rather general The arrows indicate respective <111> directions. The direction of observation is [111], the scalebar is 2µm. (d) TEM weak beam image with a high resolution zoom, clearly showing this kind of faceting is caused by horizontal twin faults on a <111> plane. The direction of observation is [0-11], the scalebar is 200 nm.*



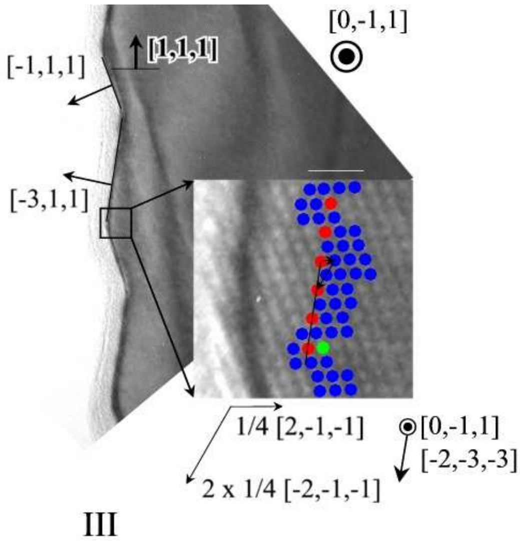


Figure II – *EDX spectra and STEM images of a silicon nanowire. An arrow indicates where the EDX spectrum has been taken. The brighter particles are unambiguously gold rich clusters, as three typical gold lines appear in the EDX spectrum around 2200 eV. The scale bar is 10 nm.*

Figure III – *High resolution TEM image showing sawtooth faceting [2]. The zoom of a small area allows identifying the alternating planes using vector calculation as shown. The viewing direction is [0-11], the scale bar is 10 nm. The alternating planes are identified as the [-111] and the [-311].*

3. Références

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