Transmission Electron Microscopy for nanometer CMOS process characterization and failure analysis

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Abstract. To remain competitive IC manufacturers have to accelerate the development of most advanced (CMOS) technology and to deliver high yielding products with best cycle times and at a competitive pricing. With the increase of technology complexity, also the need for physical characterization support increases, however many of the existing techniques are no longer adequate to effectively support the 65-45 nm technology node developments. New and improved techniques are definitely needed to better characterize the often marginal processes, but these should not significantly impact fabrication costs or cycle time. Hence, characterization and metrology challenges in state-of-the-art IC manufacturing are both of technical and economical nature. In this communication the application of TEM microscopy as a high quality, high volume analytical support is presented with practical illustrations of use in our Crolles facilities.

ELECTRON MICROSCOPY APPLICATIONS

Developers are greatly helped when they can "visualize" the as fabricated devices/creations in silicon. SEM systems have been the predominant workhorses in the Physical Characterization laboratory, but given the ever decreasing dimensions in the latest nano-CMOS technologies, are no longer capable to ensure a conclusive analysis. Especially the transition from the 180 nm to the 120 and 90 nm technology nodes has marked a spectacular and most important increase in demand for TEM analysis. Clearly, the need for information with atomic resolution has increased significantly. To reveal the chemical nature of materials, interfaces or defects, also the (S)TEM-EELS and EDX spectroscopy capabilities of the TEM microscopes are more frequently solicited. The relative ease of use and often conclusive results make the EF-TEM a 'popular application': currently almost 50 % of all TEM analyses are complemented with EFTEM or EELS.

With the shrinkage of integrated circuit dimensions into the nanometer range, the local thermo-mechanical properties of materials can more easily degrade device performance. To measure local strain at a nanometer scale, convergent beam electron diffraction (CBED) is used. Newly developed methods based on the analysis of the broadening of the high order Laue zone lines allow to estimate the stress relaxation that occurs when a sample is thinned to electron transparency and to arrive at semi-quantitative results. Finally, when device features of 30-50 nm are to be inspected with TEM, 3-D effects start to complicate the analysis. TEM tomography is under evaluation as it may be an effective way to overcome such problems and also be helpful in the detection of smallest, but yield killing defects in relatively thick TEM samples.

TEM SAMPLE PREPARATION STRATEGIES

Although its imaging and chemical analysis capabilities are excellent, a serious practical drawback of TEM microscopy is that it takes much more time than e.g. a SEM analysis, primarily because of the delicate lamella preparation process. A major challenge is, thus, to achieve high quality (S)TEM-EELS or STEM-EDX in a volume mode and with shortest cycle times. High priority is given to the development of such 'industrial' TEM line, a development that focuses on new and automated sample preparation methods. TEM lamellae are prepared in a non-destructive way via the in-situ extraction of silicon chunks from full wafers in a 300 mm FIB-SEM system followed by a final lamella preparation in a small chamber dual beam FIB-SEM system. With the latter method the device & test wafers can be re-injected in the processing flow which represents a major advantage since by doing so R&D lots can be characterized by TEM at each relevant process step and still be fully processed and electrically tested. The direct coupling between the physical information and the electrical device results of one and the same wafer ensures a much quicker and more effective learning cycle and with this method less wafers have to be processed and a step-by-step analysis can be realised in shortest time.